DETAILED ACTION

Response to Remarks

1. This Office action is considered fully responsive to the amendment filed 9/29/09.

2. The rejections under U.S.C. 101 have been withdrawn because the claims have been amended accordingly.

3. The objection to claim 7 has been withdrawn because the claim has been amended accordingly.

Response to Arguments

4. Applicant's arguments filed 9/29/09 have been fully considered but they are not persuasive.

Regarding the allegation that Ahn does not teach “comparing” because the element 104-3 does not have a comparator, but instead contains multipliers 701 and 702 (page 5, Remarks), the Examiner disagrees, as it is known that in order to perform a multiplication, the two terms involved must be compared to one another in order to produce a resulting product. In this case, the terms are compared pertaining to the mathematical operations used in multiplication, i.e. a digit of the first term is compared to another digit of the second term during the multiplication operation (a*b = “c”, where “c” depends upon the comparison of "a” and “b” in terms of multiplication rules).

Additionally, regarding the Peltier reference, Applicant argues that Peltier is used to just compare the offset between two clock signals (page 5, Remarks). It appears Applicant may have misunderstood the Examiner’s interpretation of this reference. To clarify, fig. 1 of Peltier clearly shows that there is a closed loop PLL, that contains the

phase offset elements. Col. 5, lines 10-30 describe the phase offset (in particular its sign value), interpreted as being the claimed “carrier frequency offset estimate” is compared to its prior sign (i.e. previous value), which is interpreted as being the claimed "a closed loop value of the PLL" (the previous sign is a closed loop value of the PLL), which results in checking for a false lock, or as claimed “detecting a false lock condition”.

Lastly, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* in view of U.S. Patent No. 5,490,176 to *Peltier*.

As to **claim 1**, *Ahn* discloses a method for use in a receiver, the method comprising:

using the receiver to perform the steps of:

processing a received signal with a phase-locked loop (PLL) (fig. 5, para. 0042, para. 0067, processing received signal 11, and PLL 105);

generating a carrier frequency offset estimate as a function of a phase error signal of the PLL (fig. 5, para. 0042, obtaining a phase error, and extracting a polarity of the phase error and extracting a corresponding frequency offset by making use of polarity of the phase error);

and comparing the frequency offset estimate to a closed loop value of the PLL (fig. 5, item 104-3, PLL PB_Data and oscillator with offset frequency values are inputted into frequency acquisition element).

Ahn does expressly disclose *detecting a false lock condition* as a function of comparing the frequency offset estimate to a closed loop value of the PLL.

Peltier discloses a false lock is detected when the phase offset changes sign, (abstract, col. 5, lines 10-30, claim 1), i.e. an offset signal is compared to a previous offset value.

Ahn and Peltier are analogous art because they are from the same field of endeavor regarding loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the false lock detection as taught by Peltier into the invention of Ahn. The suggestion/motivation would have been to detect false-locking of a reference signal (Peltier, col. 1, lines 5-10).

As to claim 4, *Ahn and Peltier* further discloses the method of claim 1, further comprising the step of updating the PLL with the carrier frequency offset estimate (Ahn, fig. 5, para. 0042, generating digital type sine and cosine waves according to the extracted frequency offset, these waves being part of the PLL, hence it is updated). In addition, the same suggestion/motivation of claim 1 applies.

As to **claim 5**, *Ahn* discloses a receiver (fig. 5) comprising:

a carrier tracking loop (CTL) for processing a received signal (para. 0096, specifically, two PLLs are provided in the carrier restoration section 100. For example, the carrier restoration section 100 is composed of the PLL section 104 for frequency acquisition for acquiring the frequency offset and the PLL section 105 for phase tracking for tracking the residual phase jitter);

and a processor for estimating a carrier frequency offset as a function of a phase error signal of the CTL (fig. 5, para. 0096-0097, at this time the phase/frequency detector 101 is commonly used by the PLL section 104 for frequency acquisition and the PLL section 105 for phase tracking. Also, the phase/frequency detector 101 extracts the polarity by obtaining the phase error, and then expresses the phase error by the polarity, para. 0042, extracting a corresponding frequency offset by making use of polarity of the phase error);

wherein the processor compares the frequency offset estimate to a closed loop value of the CTL (fig. 5, item 104-3, PLL PB_Data and oscillator with offset frequency values are inputted into frequency acquisition element).

Ahn does expressly disclose wherein the processor *detects a false lock condition* as a function of comparing the frequency offset estimate to a closed loop value of the CTL.

Peltier discloses a false lock is detected when the phase offset changes sign, (abstract, col. 5, lines 10-30, claim 1), i.e. an offset signal is compared to a previous offset value.

Ahn and Peltier are analogous art because they are from the same field of endeavor regarding loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the false lock detection as taught by Peltier into the invention of Ahn. The suggestion/motivation would have been to detect false-locking of a reference signal (Peltier, col. 1, lines 5-10).

7. **Claims 2-3, 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* in view of U.S. Patent No. 5,490,176 to *Peltier* and in further view of “A Digital Transmission System Using Quaternary Partial Response CPM Principle Structure and Measurement Results” to *Matzner et al.* (“*Matzner*”).

As to claim 2, *Ahn and Peltier* does not expressly disclose the method of claim 1, wherein the processing step includes the step of setting the PLL in an open loop mode of operation.

Matzner discloses on page 734, the behavior of the closed loop becomes unpredictable and a frequency offset will never be compensated, therefore a different approach is needed which uses an open-loop.

Ahn, Peltier, and *Matzner* are analogous art because they are from the same field of endeavor regarding loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the open-loop as taught by Matzner into the invention of Ahn and Peltier. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 3, *Ahn and Peltier* do not expressly disclose the method of claim 1, wherein the generating step includes the steps of:

determining a rollover count value for the phase error signal;

determining a symbol count value of the received signal;

and generating the carrier frequency offset estimate from the determined rollover count value and determined symbol count value.

Matzner discloses fig. 3, "wrap around" from max to min of phase error, page 734, "six symbols", which is a value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a symbol count value, page 734, fig. 3, "six symbols" and frequency offset changes from 2 degrees/symbol to 30 degrees/symbol, also the gradient (difference between phase error estimates, i.e. "wrap around", and since these are based on degrees per one symbol, the symbol count is

also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate phase difference per symbol, i.e. frequency offset).

Ahn, Peltier, and *Matzner* are analogous art because they are from the same field of endeavor regarding loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the various values of signals as taught by Matzner into the invention of Ahn and Peltier. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

As to claim 6, *Ahn* and *Peltier* do not expressly disclose the receiver of claim 5, wherein the CTL includes a rollover counter and a symbol counter accessible by the processor for use in estimating the carrier frequency offset.

Matzner discloses fig. 3, “wrap around” from max to min of phase error is a counted value, page 734, “six symbols”, which is a counted value pertaining to received signal, also, frequency offset is based on degrees per symbol, i.e. one symbol is also a symbol counted value, page 734, fig. 3, “six symbols” and frequency offset changes from 2 degrees/symbol to 30 degrees/symbol, also the gradient (difference between phase error estimates, i.e. “wrap around”, and since these are based on degrees per one symbol, the symbol count is also used) of the saw-tooth curve in fig. 3 is proportional to frequency offset, and this is used to estimate phase difference per symbol, i.e. frequency offset).

Ahn, Peltier, and *Matzner* are analogous art because they are from the same field of endeavor regarding loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the various values of signals as taught by Matzner into the invention of Ahn and Peltier. The suggestion/motivation would have been to compensate for unpredictable behavior (Matzner, page 734).

8. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2002/0067778 A1 to *Ahn* in view of U.S. Patent No. 5,490,176 to *Peltier* and in further view of U.S. Publication No. 2002/0122511A1 to *Kwentus et al. ("Kwentus")*.

As to claim 7, *Ahn and Peltier* do not expressly disclose the receiver of claim 5, wherein the receiver is a set-top box.

Kwentus discloses a satellite receiver in a set-top box that contains tracking loops (fig. 1, para. 0017, 0028).

Ahn, Peltier and Kwentus are analogous art because they are from the same field of endeavor regarding tracking loops.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate the set-top box receiver as taught by Kwentus into the invention of Ahn and Peltier. The suggestion/motivation would have been to recover modulated signals in a wireless communications system (Kwentus, para. 0003).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to OMAR GHOWRWAL whose telephone number is (571)270-5691. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm est..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick Ferris can be reached on (571)272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/O. G./
Examiner, Art Unit 2463

/Derrick W Ferris/
Supervisory Patent Examiner, Art Unit 2463